Advanced 3D eWLB-PoP (embedded Wafer Level Ball Grid Array - Package on Package) Technology

by

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Abstract

The emergence and evolution of any package technology is driven by market trends as experienced by the end application. With the maturation of the mobile market, the trends for Smartphone and other mobile devices are more than ever for lower cost. Meanwhile, a higher degree of functionality and performance, thinner profile, and longer battery life are some of the additional market drivers seen in these devices. The implications of these market drivers on the packaging content of mobile devices are; higher performance designs, lower cost, smaller form factor, and higher level of integration.

The advancement of silicon scaling to 14/16 nanometer (nm) in support of higher performance, higher bandwidth and lower power consumption in portable and mobile devices is pushing the boundaries of emerging packaging technologies to smaller fan-out packaging designs with finer line/spacing as well as improved electrical performance and passive embedded technology capabilities. Advanced embedded Wafer Level Ball Grid Array (eWLB) technology provides a versatile platform for the semiconductor industry's technology evolution from single or multi-die 2D package designs to 2.5D interposers and 3D System-in-Package (SiP) configurations.

Earlier in 2012, eWLB Package-on-Package (eWLB-PoP) technology delivered a 30% height reduction in PoP, reducing the overall stacked package height from the industry standard 1.4mm to 1.0mm. Through further innovations in eWLB technology, a 40% height reduction in the bottom PoP architecture has been achieved. An ultra thin z-height of 0.3mm was realized in 2013, thereby providing the advantage of having an overall PoP package height as low as 0.8mm with proven board level reliability. While traditional PoP solutions are widely used in the high-end mobility market, demand is accelerating for ultra thin, cost effective packages that have the flexibility to serve a range of applications from mid-range to low-end mobile phones as well as tablets that require significantly higher processor speeds. While printed circuit board (PCB) substrate technology limits the interconnection density of a PoP package to 200-300 input/output (I/O), eWLB-based PoP solutions can deliver beyond 500 I/O in an overall thinner package with a dense vertical interconnection and wider interfap 0 n witi(gwi)2eTkobile ed cibile pwi

requirement for lower cost and power consumption. The challenge for the semiconductor industry is to develop a disruptive packaging technology capable of achieving these goals.

To meet the above said challenges, eWLB is a continually evolving technology platform which offers additional space for routing higher I/O chips on top of the silicon (Si) chip area which is not possible in conventional wafer level packaging (WLP) or wafer level bump (WLB) [1]. It also offers comparatively better electrical, thermal and reliability performance at a reduced cost with the possibility to address more Moore (decreasing technology nodes with low-k dielectrics in SoC) and more than Moore (heterogeneous integration of chips with different wafer technology as SiP solution in multi die or 3D eWLB approaches) as shown Fig. 1(b).

eWLB technology uses a combination of front- and back-end manufacturing techniques with parallel processing of all the chips on a wafer, which can greatly reduce manufacturing costs. Its benefits include a smaller package footprint compared to conventional leadframe or laminate packages, medium to high I/O count, maximum connection density, as well as desirable electrical and thermal performance. It also offers a high-performance, power-efficient solution for the wireless market [2].

(a)

(b)

Figure 1. (a) 300mm eWLB carrier and eWLB packages, and (b) evolution of eWLB technology from 2D to 2.5D/3D packaging solution

eWLB (embedded Wafer Level BGA) Technology

eWLB technology is addressing a wide range of factors. At one end of the spectrum is the packaging cost along with testing costs. Alongside, there are physical constraints such as its footprint and height. Other parameters that were considered during the development phase included I/O density, a particular challenge for small chips with a high pin count; the need to accommodate SiP approaches, thermal issues related to power consumption and the device's electrical performance (including electrical parasitic and operating frequency) [3]. The obvious solution to the challenges was some form of WLP. Two choices presented themselves: Fan-in or Fan-out. With Fan-in WLP or Wafer Level Chip Scale Packaging (WLCSP), the I/O density is limited to the die size. In Fan-out WLP (FO-WLP) or eWLB,, the interconnection system is processed directly on the wafer and the I/O density is unconstrained by die size, making it compatible with motherboard technology pitch requirements.

The wafer level chip scale package (WLCSP) was introduced in the late 1990's as a semiconductor package wherein all manufacturing operations were done in wafer form with dielectrics, thin film metals and solder bumps directly on the surface of the die with no additional packaging[1]. The basic structure of the WLCSP has an active surface with polymer coatings and bumps with bare silicon (Si) exposed on the remaining sides and back of the

2) The singulated die are accurately placed face down onto the carrier with a pick and place tool.
3) A compression molding process is used to encapsulate the die with molding compound while the active face of the die is protected.
4) After curing the molding compound, the carrier and foil are removed with a de-bonding process, resulting in a reconstituted wafer where the molding compound surrounds all exposed silicon die surfaces.

The eWLB process is unique in that the reconstituted wafer does not require a carrier during the subsequent wafer level packaging processes. The implementation of this process flow into 300mm diameter reconstituted wafers has been described in detail in previous presentations [2].

3D eWLB-PoP Technology

The continued demand for higher level of integration has led to the industry's adoption of 3D packaging technologies and, in particular, the Package-On-Package (PoP) configurations. This technology allows for vertical integration of the memory package and the logic package into one stacked package.

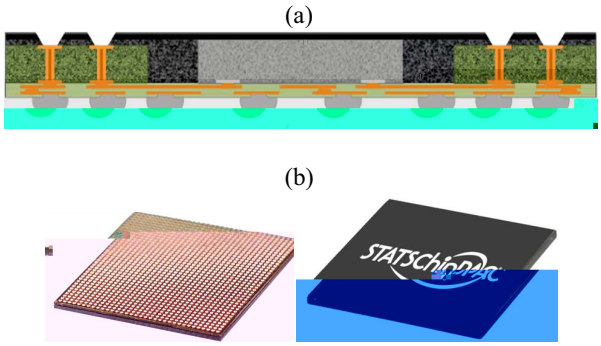

Figure 3. (a) Schematics of package structure of 3D eWLB-PoP bottom and (b) 3D eWLB-PoP stacked (with top memory package) of total 0.8mm height.

The top package is primarily a memory module including some combination of Flash and DRAM, while the bottom package typically contains the logic die, which is a baseband or an application processor of some kind. Top and bottom package are connected via the pads that are located on the top side of the bottom PoP package, and these pads are used to connect the top PoP (memory module) Ball Grid Array (BGA) solder balls to the bottom PoP package. There are various PoP package types including bare-die PoP, Embedded Solder On Pad (eSOP) PoP, and Laser-Via PoP that have proliferated to meet the increasing market demand [4].

3D eWLB-PoP offers significant advantages in thin profiles and lower cost compared to current PoP technologies, particularly for mobile or tablet applications. 3D eWLB-PoP bottom has a 300um package height enabling a total stacked PoP height to be less than 0.8 mm after top memory package stacking (body thickness of 0.40mm). Table 1 shows value proposition of 3D eWLB-PoP technology.

Table 1. Value proposition of eWLB-PoP

1.	*15 15*
2.	*0.8 (300).*
3.	*0.6*
4.	
5.	
6.	
7.	*0.2 (1000 , 16 16)*
8.	-

II. Experimental Results

3D eWLB-PoP Test Vehicle Specification

For further process development and reliability tests, two test vehicles were designed as shown in Table 2. Both packages were used for further component/board level reliability tests with ball shear and open-short (OS) tests. For TV2, the specification was used for thermal characterization with thermal die assembly. In addition, the 28nm fab-node functional devices of TV1 and TV2 were assembled for electrical functional characterization and compared to a flip chip PoP (fcPoP).

Table 2. eWLB-PoP Test Vehicles Specification

	TV1	TV2
Package body size	10x10mm	15x15mm
Die size	50mm^2	110mm^2
Ball IO	~400	~1000
Top ball pitch	0.4mm	0.35mm
Bottom ball pitch	0.4mm	0.4mm
Ball size	0.25mm	0.25mm
Body thickness	0.2mm	0.20mm

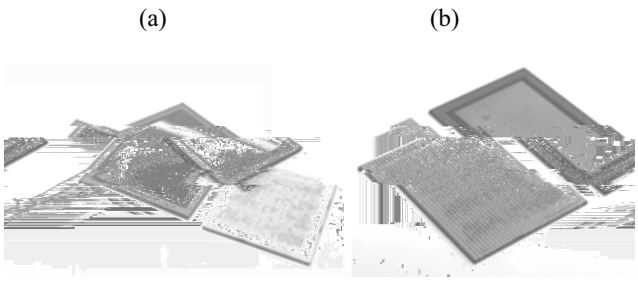

Figure 4. Micrograph of 3D eWLB-PoP; (a) TV1 and (b) TV2

Component Level Reliability of 3D eWLB-PoP

Table 3 shows the package level reliability result of 3D eWLB-PoP. They passed JEDEC (Joint Electron Device Engineering Council) standard package reliability tests such as MSL (Moisture Sensitivity Level) 3 with Pb-free solder conditions. The test vehicles (TV1/2) were 10x10mm and 15x15mm 3D eWLB-PoP. Both successfully passed all industry standard package level reliability with ball shear test and OS test.

Table 3. Package Level Reliability Results of 3D eWLB-PoP.

Reliability Test	JEDEC	Test Condition	Read-out	Results
Unbiased HAST (W/ MSL3)	JESD22-A118	130°C, 85%RH	168hrs	Pass
Temperature Cycling (TC-B, w/MSL3)	JESD22-A104	-55/125°C; 2Cy/hr	1000x	Pass
High Temp. Storage (HTS)	JESD22-A103	150°C	1000hr	Pass

Experimental Thermal Characterization of 3D eWLB-PoP

For thermal characterization, the test vehicle was prepared with thermal die. Test vehicle specification was same as TV2 in Table 2(b). In this study, die thickness effect was studied with 3 different die thicknesses: 200um, 300um and 400um. The same die sizes for fcPoP were prepared for the comparison study.

All test vehicles had thermal die with a transistor and heating circuit block as well as temperature sensor so it easily detected temperature at the hot spot of the die with applied power. After SMT on thermal test PCB, 2.0W power was applied and measured junction temperature with various die thickness. As shown in Figure 5, eWLB-PoP has 8-10% thermal performance improvement for the same die thickness as compared to fcPoP. For eWLB, it can use thicker die than fcPoP for embedding, achieving a >20% improvement in thermal performance with the same package height of eWLB-PoP compared to fcPoP.

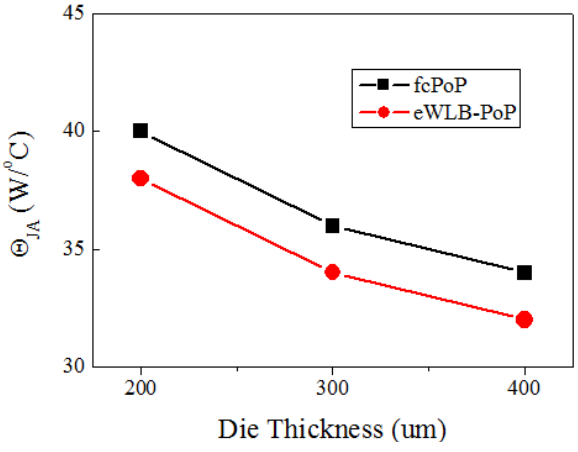

Figure 5. Thermal characterization data of 3D eWLB-PoP with different die thickness compared to fcPoP.

Electrical Functional Characterization of 3D eWLB-PoP

The TV1 and TV2 were assembled with Live dice from 28nm Low Power Foundry technology. After assembling the 3D eWLB PoP, final functional test, bench test and system level test (SLT) were performed with existing test infrastructure including test hardware of fcPoP. Test was also carried out at room temperature and hot-test of 110°C. Both TV1, TV2 passed SLT testing and all Stress tests (MSL3,TC, HTS) as shown in Table 3.

Test data shows 3D eWLB-PoP performance is equivalent or slightly improved compared to fcPoP solutions. Multiple retests did not result in cracking and it proved the mechanical robustness of low profile 3D eWLB-PoP.

Parasitic Electrical Simulation of 3D eWLB-PoP and fcPoP

The RLC parasitic values for eWLB-PoP and fcPoP were extracted by computer simulation using commercial 2D electromagnetic field solver. The S-parameter of each packages were extracted by using ANSOFT HFSS. Simulated results are compared with RLC parasitic values and S parameters. The simulation modeling design was carried out with functional devices to investigate package level performance in real applications. In 3D simulation works, a few critical pins were selected and studied, such as clock, VDD as well Data pins.

Table 4. Electrical parasitic values of RL of eWLB-PoP and fcPoP @ 1GHz. :

Net	Inductance, L (nH)			Resistance, R (mΩ)		
	fcPoP	eWLB -PoP	Δ (%)	fcPoP	eWLB -PoP	Δ (%)
1	1.77	0.43	-76%	240	67	-72%
2	2.03	0.24	-88%	308	42	-86%
3	1.51	0.57	-62%	348	112	-68%
4	1.08	0.25	-77%	268	66	-75%

Board Level Reliability of 3D eWLB-PoP

For board level reliability tests, eWLB-PoP (stacked with top package) was assembled and mounted on the PCB. For PoP assembly, 0.4mm body thickness FBGA top packages were assembled and the total eWLB-PoP stacked package was less than 0.8mm in height after SMT on PCB. Those samples were tested in JEDEC TCoB and drop reliability test conditions.

Table 4 shows 3D eWLB-PoP board level reliability of JEDEC TCoB and drop test results of test vehicle 1 and 2 (Table 2 and Figure 3). The first TCoB failure was after 1000 cycles. Drop reliability performance was robust and showed no failure after 300 drops. These test results show the robustness of board level reliability of 3D eWLB-PoP.

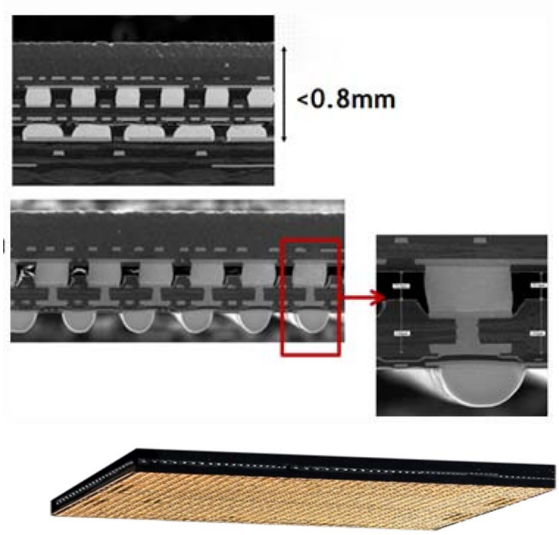

Figure 6. Micrographs of cross-section of 3D eWLB-PoP stacked after top package attachment.

Table 4. Board Level Reliability Test Results of 3D eWLB-PoP

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40°C to 125°C	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass

3D eWLB SiP / Module

FO-WLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP integration is also a growing trend for advanced application processors, MEMS and sensors in IoT/WE as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor[5].

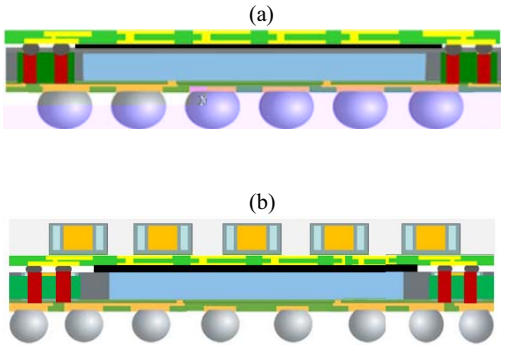

Figure 7. Schematics of 3D eWLB SiP: (a) with interposer and (b) discretes on interposer or top package of discretes.

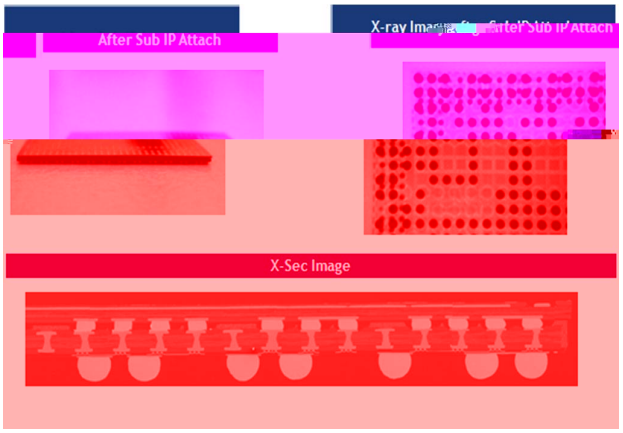

Figure 8. Micrographs of 3D eWLB SiP with interposer

Figure 7 shows one of example of 3D eWLB SiP/module which that has a number of discretes in the top package and is pre-stacked on the bottom eWLB to form a 3D SiP/ module with a thin profile. Discretes were removed from the motherboard and relocated in the top package for a reduction in the space required on the mother board. Discretes are also more effective when they are close to the device, which significantly improves the overall performance as well as provides a power saving advantage.

Functional test samples were prepared as shown in Figures 8 and 9, respectively. For Figure 8, a 15x15mm eWLB-PoP was assembled as described and a thin substrate with bump was attached on top of eWLB-PoP. The total height is was less than 0.5mm. In addition, the Figure7(b) concept was demonstrated as shown in Figure 8 9. It was a 6x6mm package size with a 4x4mm Si die and 12 discretes on top. This 3D eWLB SiP demonstrated more attractive power efficiency performance compared to conventional packaging and it is representative of a significantly smaller packaging solution that is well-suited for IoT or WE devices.

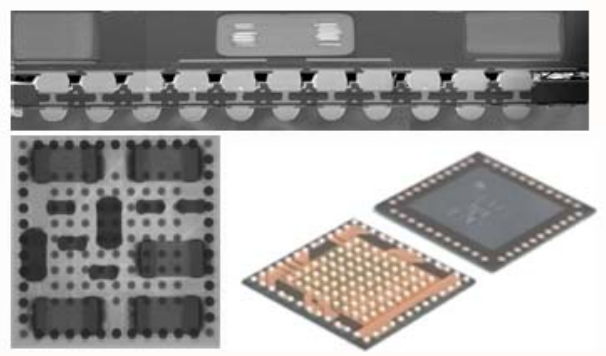

Figure 9. Photographs of 3D SiP eWLB-PoP with discretes on interposer or top package of discretes.

III. Conclusions

Rapid growth of mobile and emerging IoT/WE devices will be enabled only by more compact and low-cost

semiconductor packages with increased performance and packaging complexity. Wafer level technology effectively accommodates new ~~lithography~~ foundry technology nodes and provides a strong packaging platform to address performance, form factor, integration and cost requirements. In addition to providing higher bandwidth, ultra high density, embedded capabilities, and improved thermal dissipation in a small, thin package format, advanced wafer level packaging is an alternative for small flip-chip and large QFN packages and is quickly becoming a package of choice in the evolving mobile, IoT and WE markets. Fan-out wafer level technology also provides the ability to tightly manage the co-design process and achieve silicon optimization, which is increasingly important in ultra cost-sensitive markets.

Advanced packaging plays a crucial role in delivering achieving higher performance, lower power, lower cost, and a smaller form factor. There are many challenges that have been, and are being resolved in the application of cost-effective materials and processes for various reliability and security requirements for new and emerging mobile, IoT and WE applications. The industry requires innovation in packaging technology and a cost-effective, high-volume manufacturing process that is able to meet current and forecasted market demands.

eWLB technology is an important wafer level packaging solution that will enable the next generation of mobile applications. The advantages of standard fan-in WLPs, such as low assembly cost, minimum dimenrryr varioa BT . 2 Tc Tw TL . . 2 .25 5 . 3 m 52 r power,TJrxmce(s tt elhi)r. Tl